

SYSTEM BUS

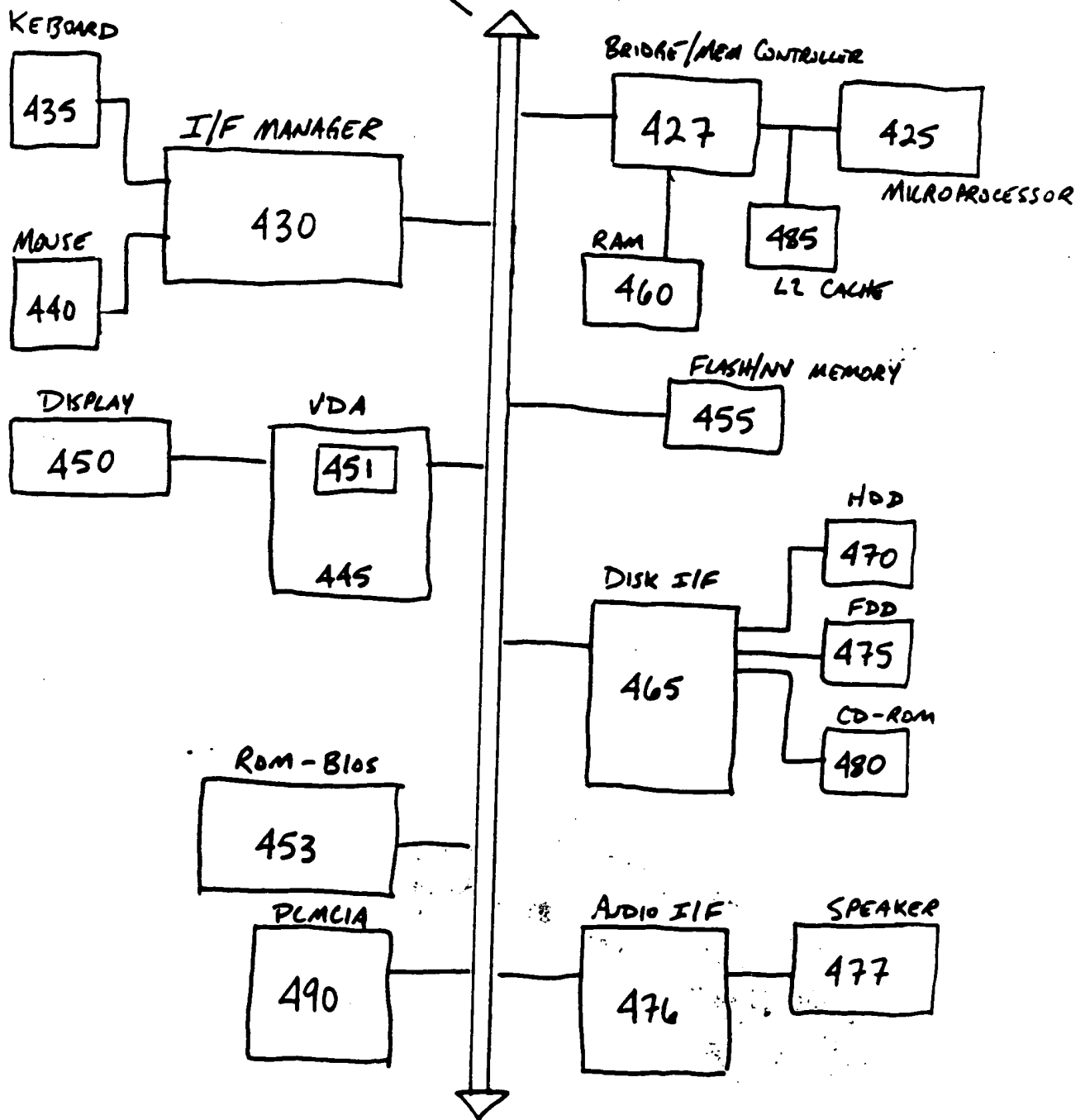
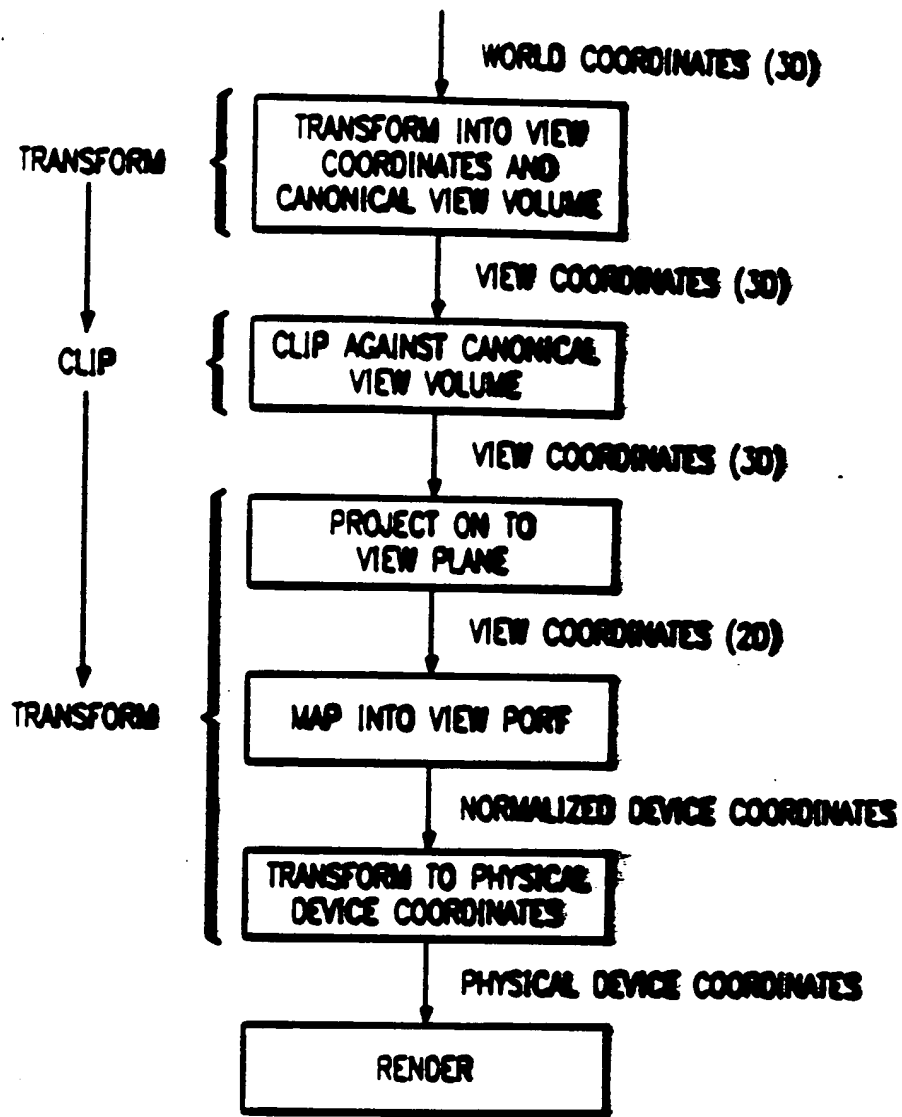


FIG 1

FIG. 2



The diagram illustrates the internal architecture of the S3 86C453 graphics chip. At the top, the chip is connected to **SGRAM / SDRAM** via a **Memory Interface Unit**. This unit also manages data flow between the **2708Kbit RAMDAC** and the **2D, 3D and Video Graphics Core**. The **RAMDAC** outputs **R**, **G**, and **B** color signals and is controlled by **DDC2AB**. The **Graphics Core** includes a **Rendering Subsystem** and a **Pipeline Set-up Processor**. It interfaces with **DMA 2** and **DMA 1** units, which connect to the **PCI / AGP Interface** at the bottom. This interface is linked to a **PCI / AGP Bus Connector**. On the right side, the chip features a **Video Stream Interface** that connects to external components: **SDRAM ROM**, a **General Purpose Bus**, **Video Port 1** (leading to **NTSC PAL**), **Video Port 2** (leading to **TV Tuner**), and a **DIC** output.

Figure 3

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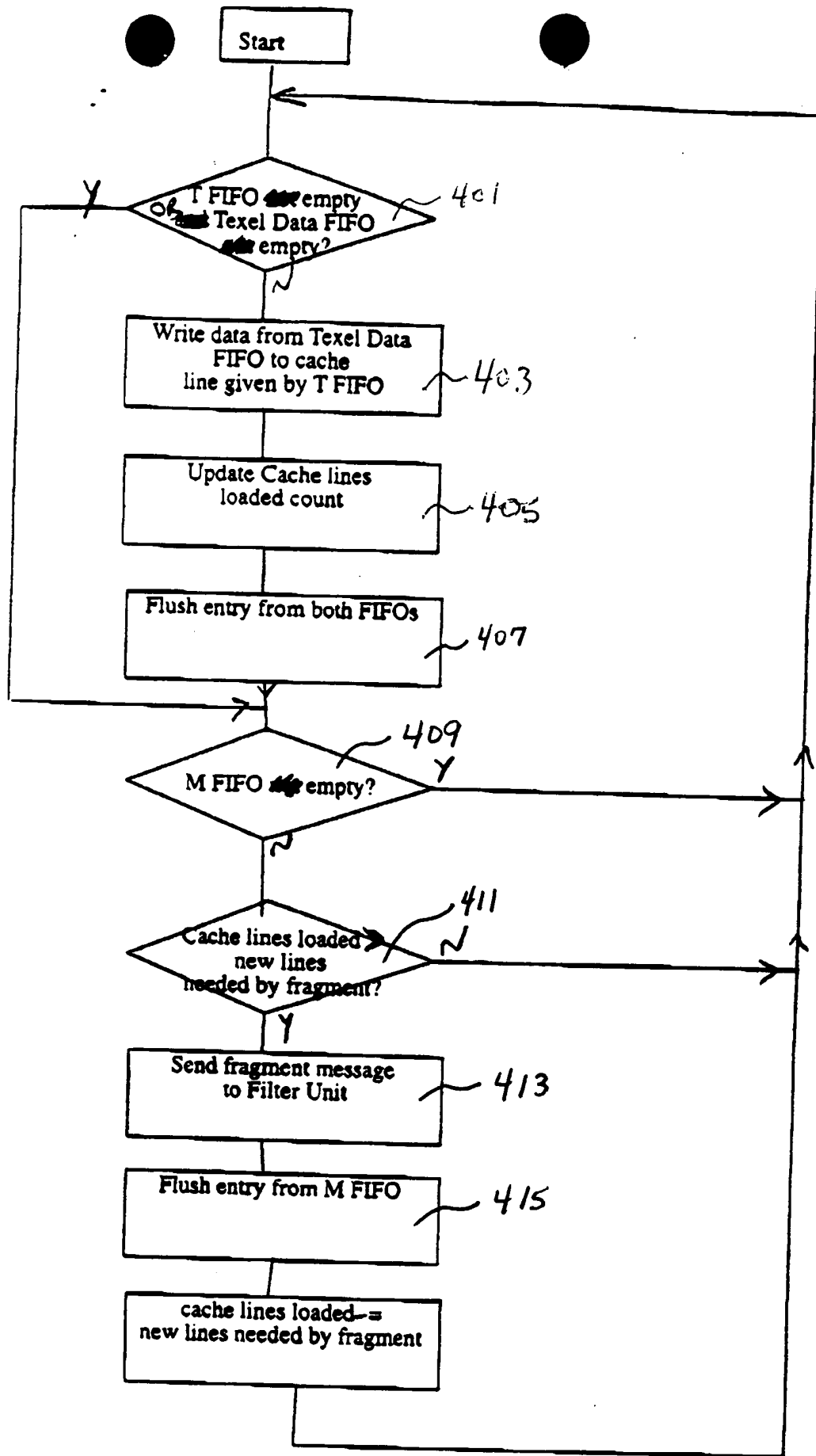


FIG. 4A

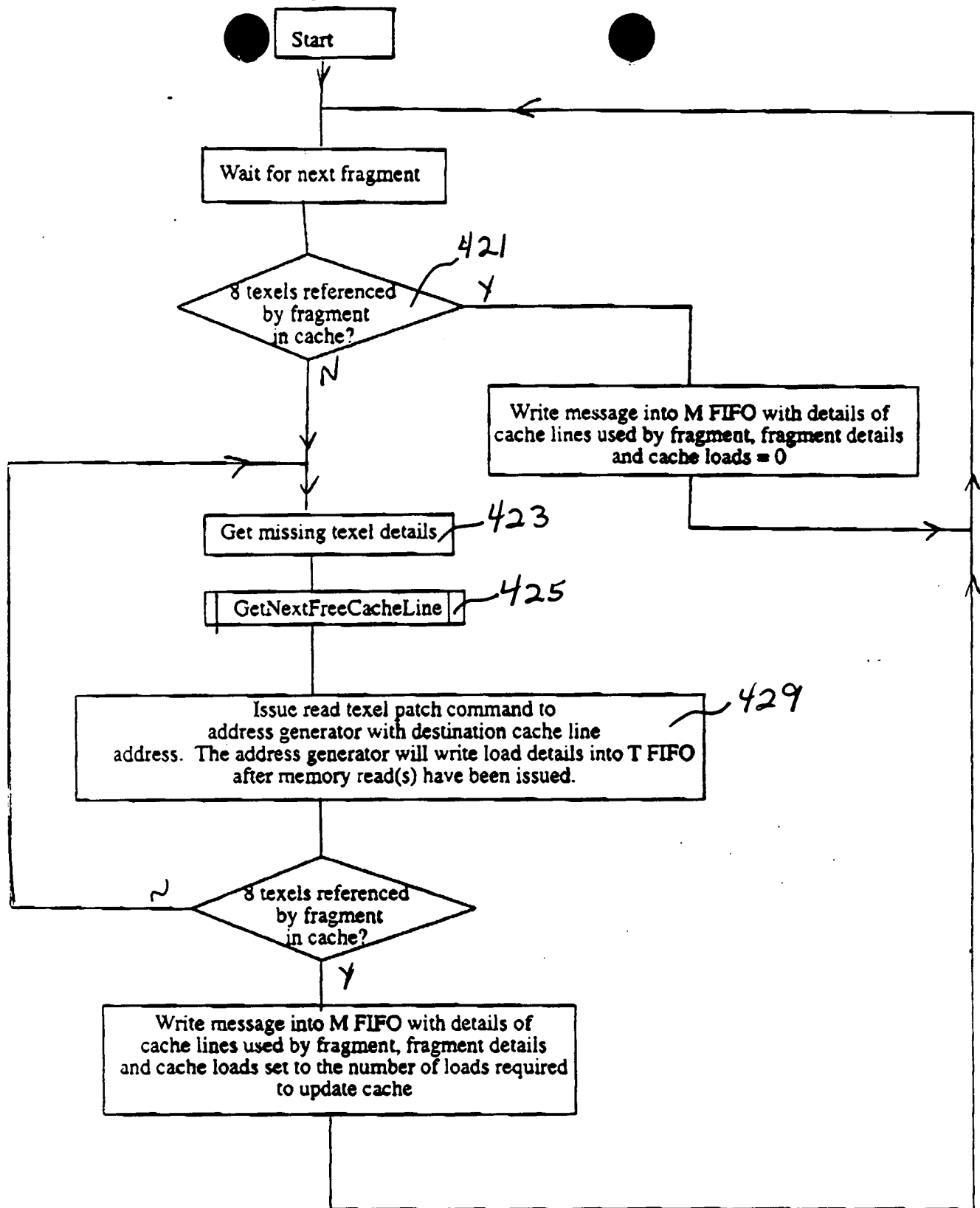


FIG 4B

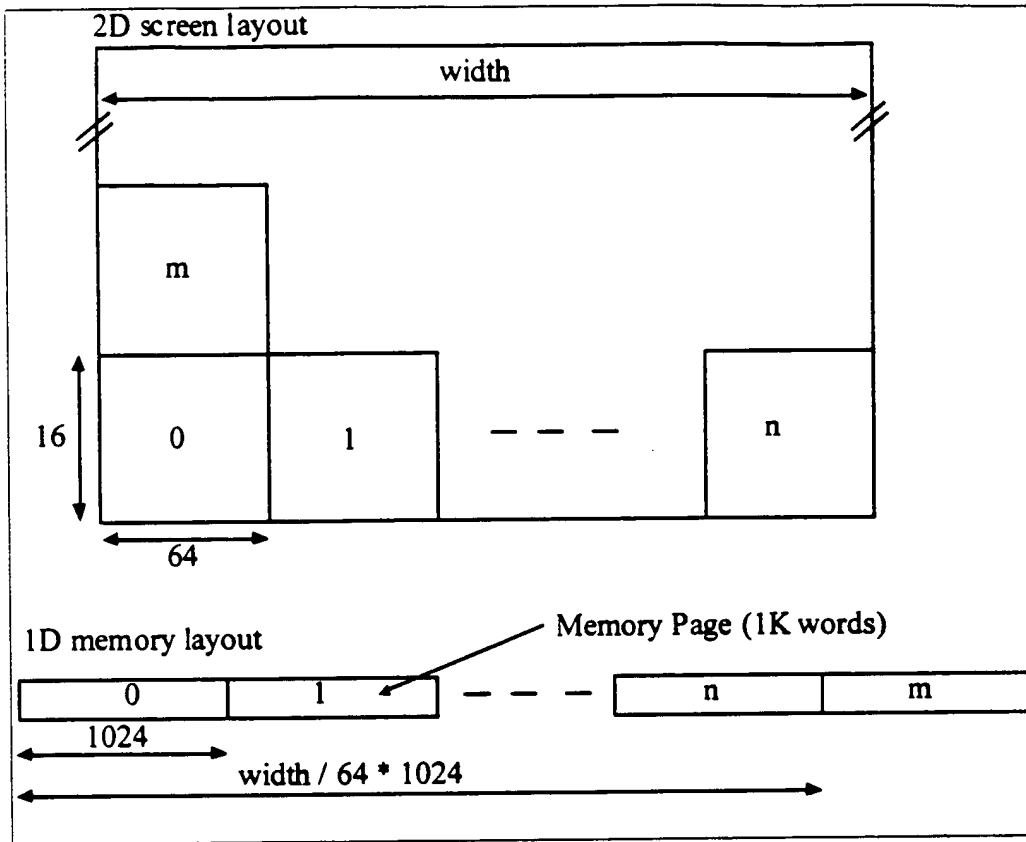


FIG. 5

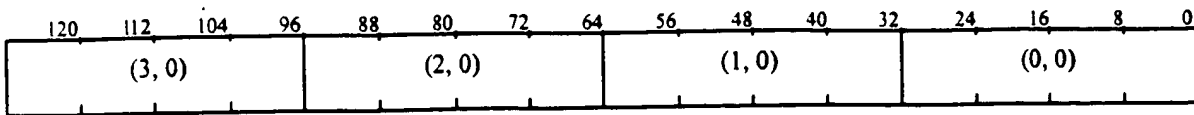
T0 (0,4)	T1 (1,4)	T0 (2,4)	T1 (3,4)	T0 (4,4)	T1 (5,4)	T0 (6,4)	T1 (7,4)	T0 (8,4)	T1 (9,4)
T2 (0,3)	T3 (1,3)	T2 (2,3)	T3 (3,3)	T2 (4,3)	T3 (5,3)	T2 (6,3)	T3 (7,3)	T2 (8,3)	T3 (9,3)
T0 (0,2)	T1 (1,2)	T0 (2,2)	T1 (3,2)	T0 (4,2)	T1 (5,2)	T0 (6,2)	T1 (7,2)	T0 (8,2)	T1 (9,2)
T0 (0,1)	T1 (1,1)	T2 (2,1)	T3 (3,1)	T2 (4,1)	T3 (5,1)	T2 (6,1)	T3 (7,1)	T2 (8,1)	T3 (9,1)
T0 (0,0)	T1 (1,0)	T2 (2,0)	T3 (3,0)	T2 (4,0)	T3 (5,0)	T2 (6,0)	T3 (7,0)	T2 (8,0)	T3 (9,0)

- 32 bit texels in memory word
- 16 bit texels in memory word
- 8 bit texels in memory word

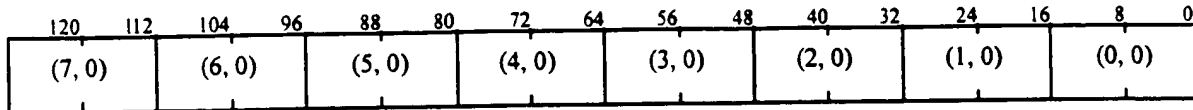
FIG. 6

Linear or Patch64 Memory Layouts

32 bits per texel



16 bits per texel



8 bits per texel

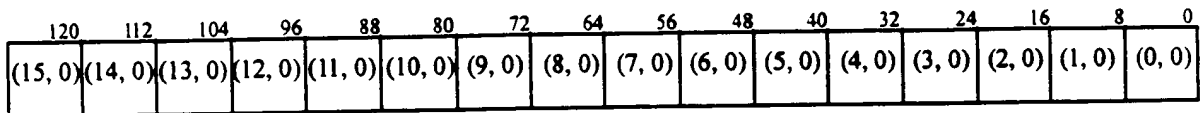
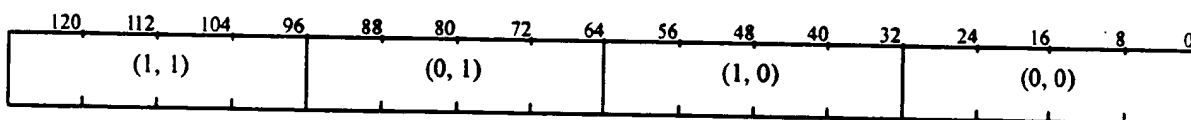


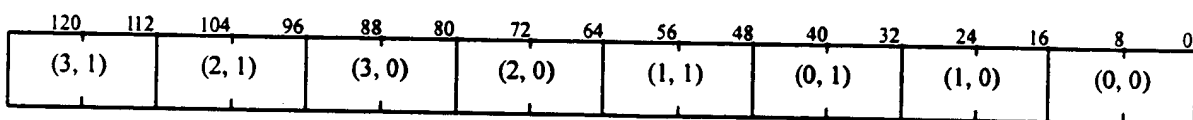
FIG. 7A

Patch32_2 or Patch2 Memory Layouts

32 bits per texel



16 bits per texel



8 bits per texel

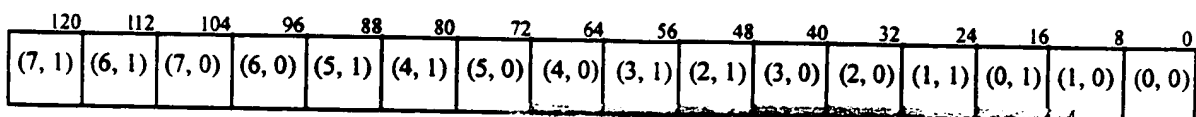


FIG. 7B

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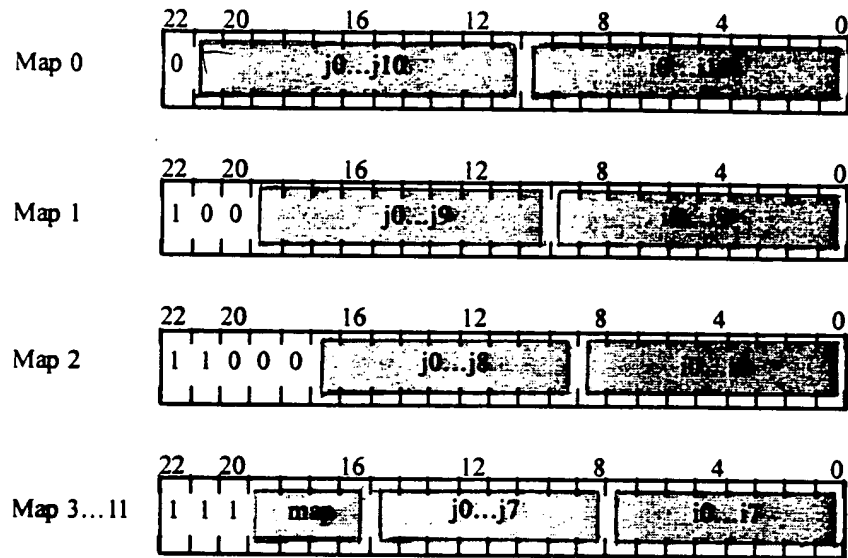


FIG. 8

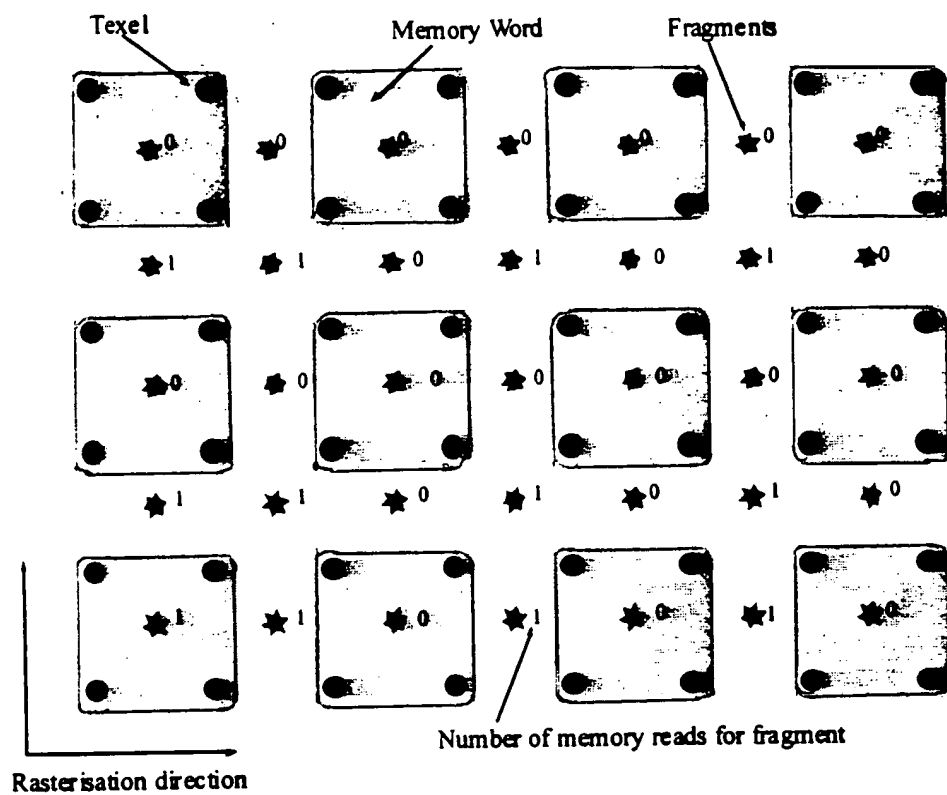


FIG. 9

Figure 6-10: Detailed Block Diagram of the Texture Unit

The diagram illustrates the internal architecture of the texture unit, showing the flow of data and control signals between various components.

Key Components and Connections:

- Download Controller:** Receives data from the PCI Bus via a Texture Input FIFO [16] and outputs to the Memory Controller via a Tx Wr FIFO [8]. It also manages MAC and MAD FIFOs [16] and interacts with the Memory Allocator.
- Memory Controller:** Manages memory operations, receiving address/data [128] and outputting address/data [64] and data [128]. It interfaces with the Memory Allocator and the Address Mapper.
- Memory Allocator:** Manages physical pages, outputting PhysicalPage [16] to the TLB I FIFO and InvalidPage [16] to the TLB D FIFO. It also receives commands from the Address Mapper.
- TLB (Translation Lookaside Buffer):** Consists of TLB I FIFO, TLB D FIFO, and TLB C FIFO. It stores valid physical pages and provides information to the Address Mapper.
- Address Mapper:** Maps virtual addresses to physical addresses, receiving commands from the Memory Allocator and outputting address/data [28] Logical Filter to the Address Generator.
- Address Generator:** Generates addresses based on commands (only AG0), i[12], j[12], map[12], filter[1], and cacheLine[8]. It outputs address/data [32/64] P3/RX to the T FIFO.
- Primary Cache Manager:** Manages the primary cache, receiving data from the Texture Index Unit and outputting message tag and data (11+217) to the M FIFO.
- Dispatcher:** Dispatches data to the Texture LUT Unit, receiving data from the M FIFO and outputting Tag[11], Data[203], LoadEnable[1], LoadAddr[9], and LoadData[128].

FIFOs and Buffers:

- Tx Wr FIFO [8]: Transaction write buffer.
- MAR FIFO: Memory Access Register buffer.
- Tx Addr0 FIFO, Tx Addr1 FIFO: Transaction address buffers.
- Tx Data0 FIFO, Tx Data1 FIFO: Transaction data buffers.
- AM FIFO [8]*: Address Mapper buffer.
- T FIFO [32/64] P3/RX: Texture FIFO.
- M FIFO [32/64] P3/RX: Message FIFO.
- AG0 FIFO [8], AG1 FIFO [8]: Address Generator buffers.

Commands:

- TextureDownloadRequest
- TextureDownloadingProgress
- DownloadLogicalPage[16]
- TextureDownloadComplete
- InvalidatePage
- InvalidateTable
- InTLB
- NewTLBEntry + Data[32]
- MostRecentPage
- RemoveLogicalReference + data[16]

PCI Registers:

- paiHostTextureAddr
- paiLogicalTextureAddr
- paiTextureOperation
- paiTextureDownloadRequest

Note: FIFOs are 1 deep unless noted. FIFOs marked * may be less deep for P3.

To Texture LUT Unit:

- Tag[11]
- Data[203]
- LoadEnable[1]
- LoadAddr[9]
- LoadData[128]

To Texture LUT Unit:
Tag[11]
Data[203]
LoadEnable[1]
LoadAddr[9]
LoadData[128]

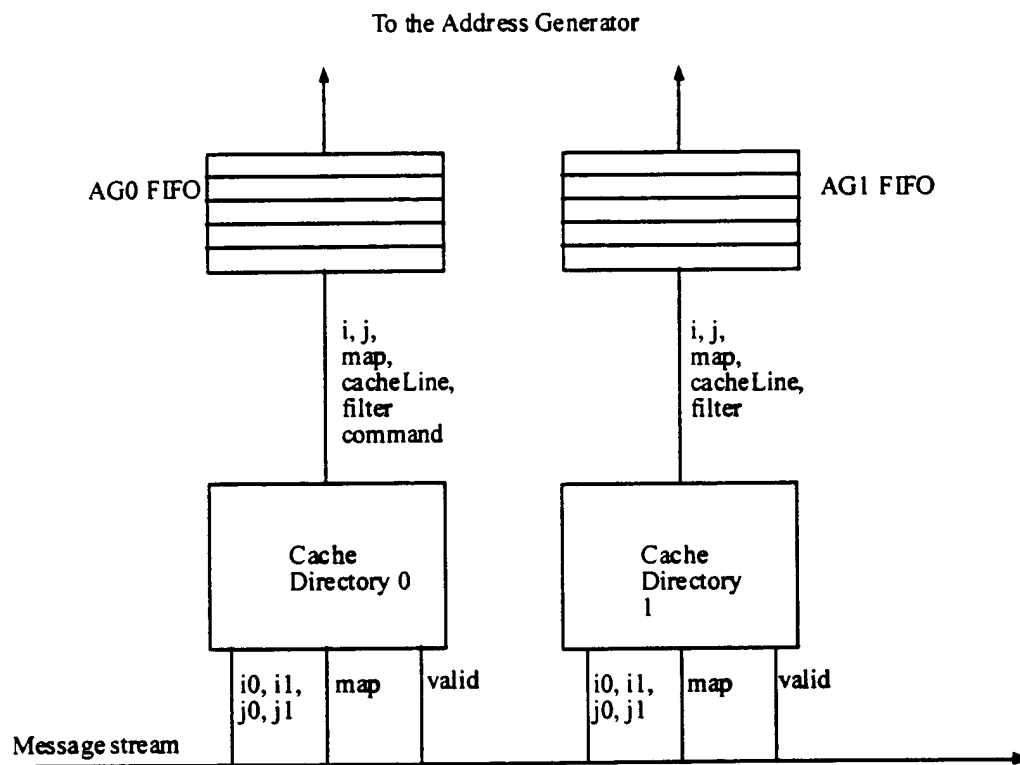


FIG. 11

The diagram illustrates a CAM (Content-Addressable Memory) architecture. It features a central CAM array with rows labeled 0, 1, 2, ..., 63 (P3) and 255 (RX). Each row is connected to a CAM Cell. The CAM Cells are connected to a multiplexer (mux) which outputs LoadData, LoadEnable, and Invalidate signals. The CAM array is also connected to a cache array with multiple rows (0, 1, 2, ..., 63) and columns (cacheAddr0, cacheAddr1, cacheAddr2, cacheAddr3). The cache array is connected to a multiplexer (mux) which outputs LoadData, LoadEnable, and Invalidate signals. The CAM array is also connected to a cache array with multiple rows (0, 1, 2, ..., 63) and columns (cacheAddr0, cacheAddr1, cacheAddr2, cacheAddr3). The cache array is connected to a multiplexer (mux) which outputs LoadData, LoadEnable, and Invalidate signals.

FIG 12

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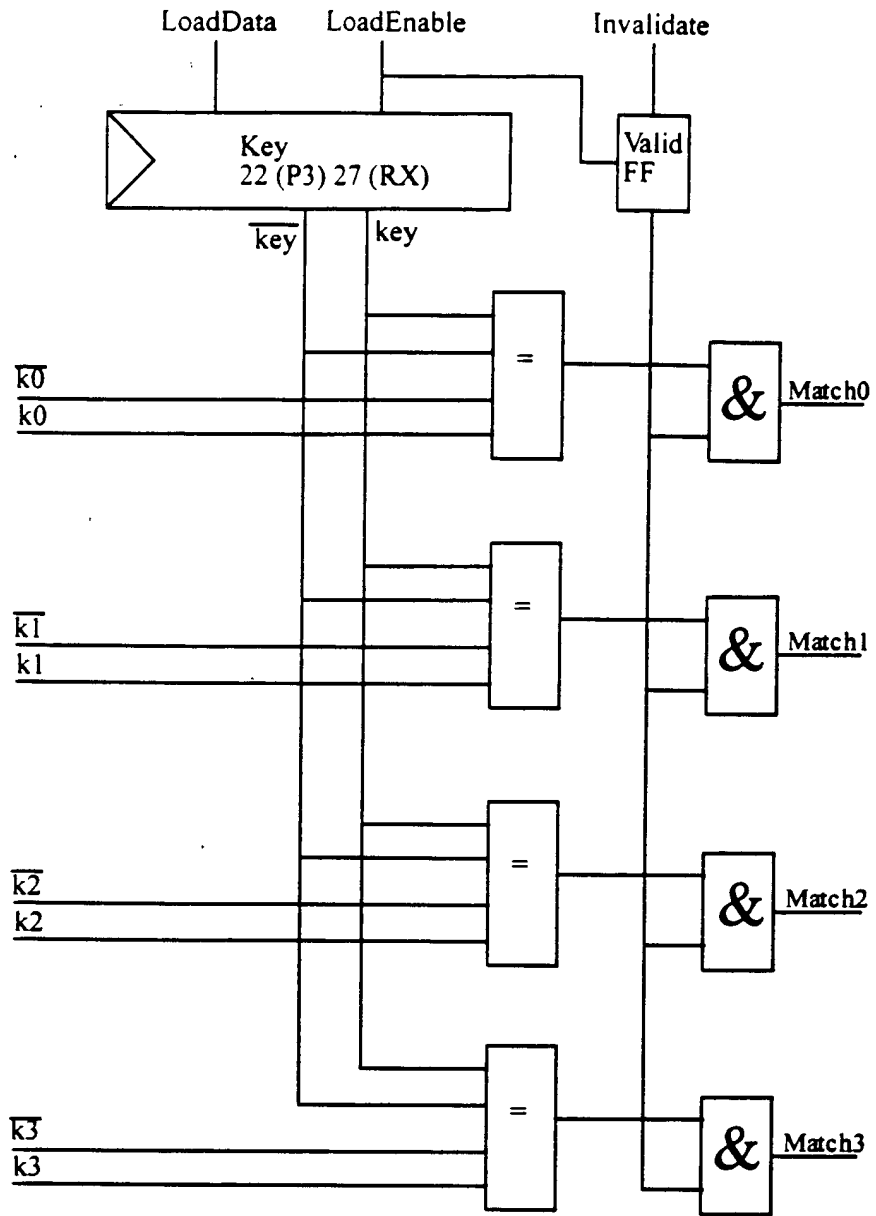


FIG. 13

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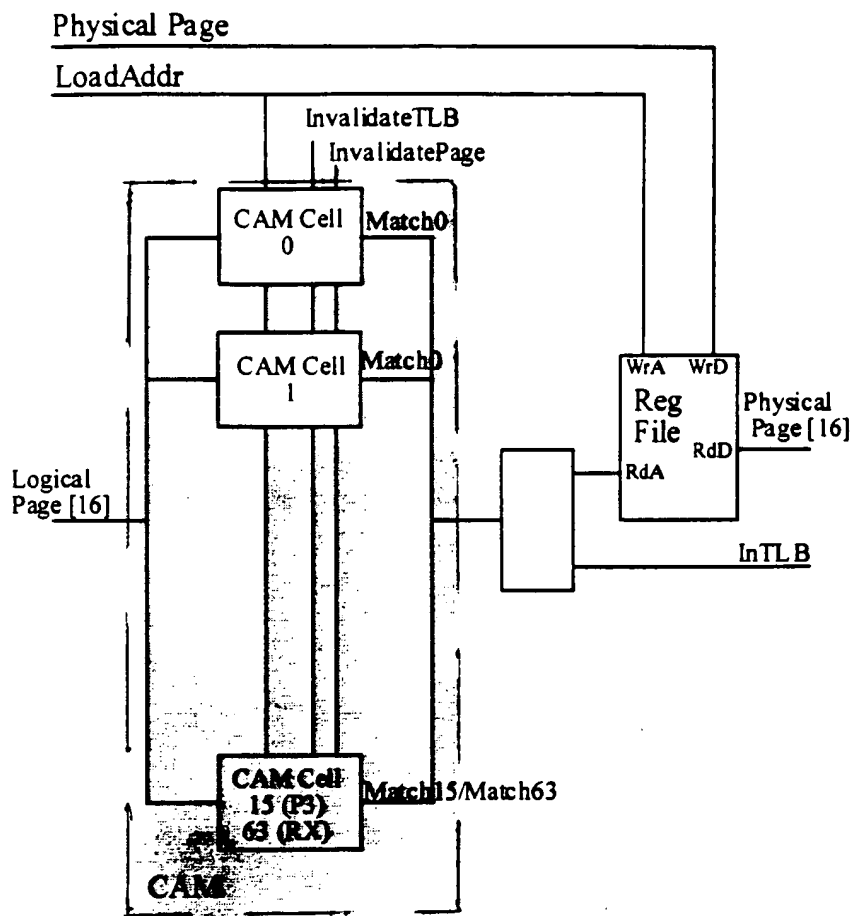


FIG. 14

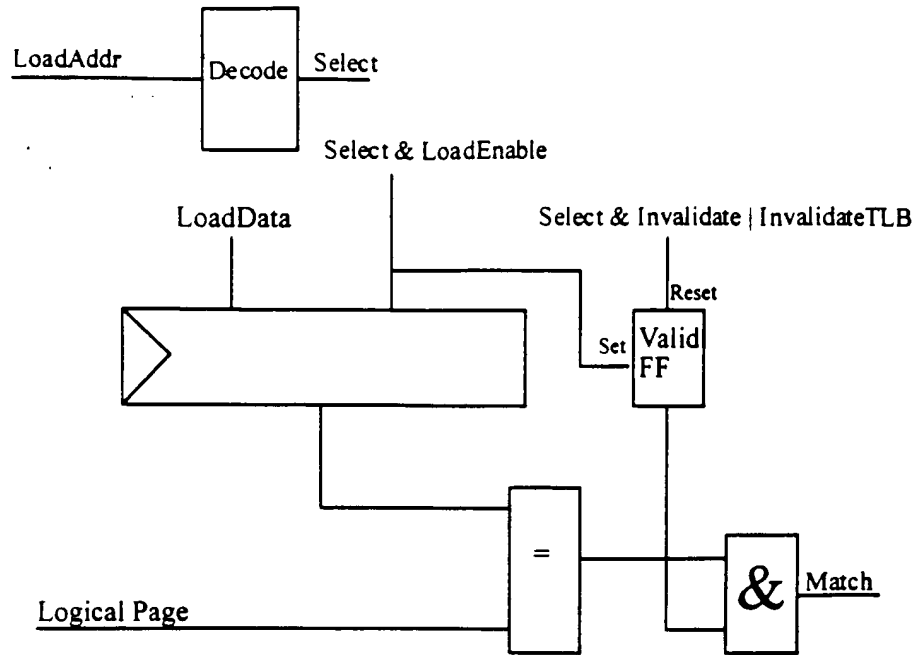


FIG. 15

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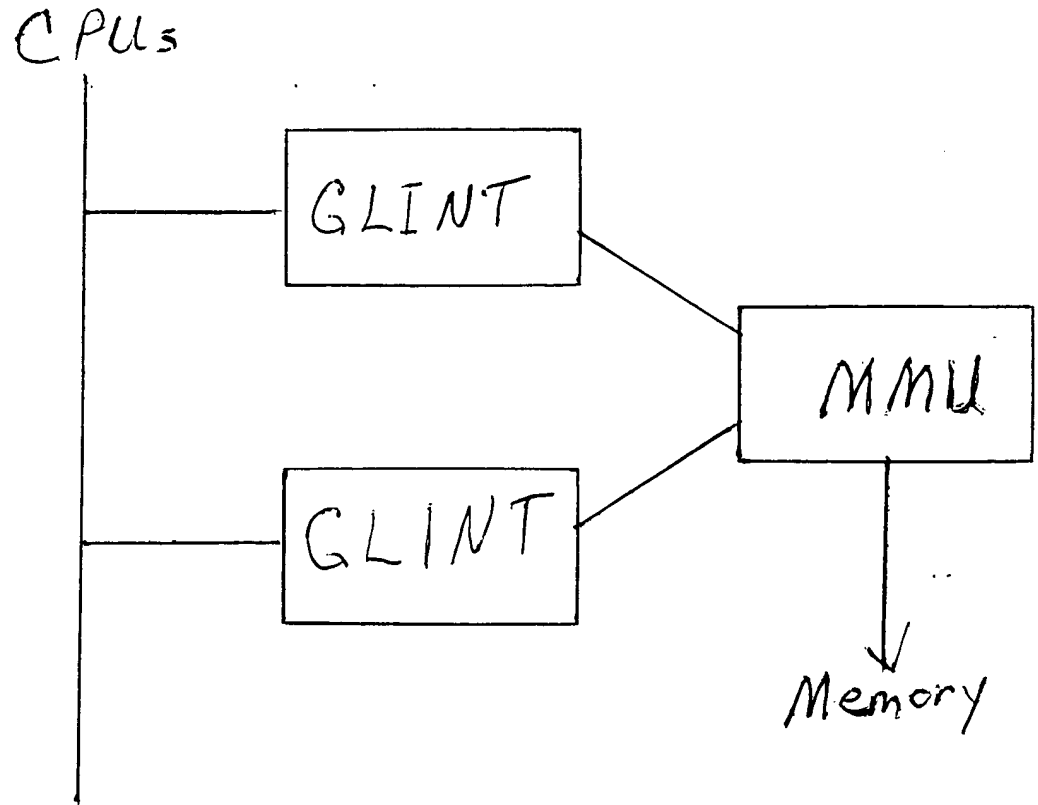


FIG. 16